PAT-NO:

-A <sup>a</sup> . j

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TITLE:

CLOCK FAULT PROCESSING SYSTEM

PUBN-DATE:

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INVENTOR-INFORMATION:

NAME

NAKAMURA, AKIHIKO

ASSIGNEE - INFORMATION:

NAME

COUNTRY

KOUFU NIPPON DENKI KK

N/A

APPL-NO: JP01047540

APPL-DATE: February 28, 1989

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## ABSTRACT:

PURPOSE: To shorten the time required for investigating a fault cause by permitting clock fault detection circuits to detect clock abnormality and permitting a fault processing program to log a clock fault occurrence phenomenon and a clock fault occurrence part.

CONSTITUTION: When abnormality occurs in a clock supplied from a clock distribution circuit 5 to processors 1-3 through clock signal lines 111-113, 121-123 and 131-133, the clock fault detection circuits 61-63 detect it, and inform an interruption signal generation circuit 7 of it through signal lines 141-143. The processor where the clock fault has occurred is recognized and a fault processing control part 82 executes the designated fault processing program by permitting the interruption signal generation circuit

7 which has received information to generate an interruption signal so as to interrupt it into a maintenance diagnosis processor 8 and permitting an interruption processing control part 81 to read a status read register 71. Thus a clock fault processing can be executed in a short time.

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